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Norris

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[54] **DYNAMIC PROCESSOR PERFORMANCE AND POWER MANAGEMENT IN A COMPUTER SYSTEM**

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Related U.S. Application Data

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[51] **Int. Cl.**[6] **G06F 13/00**

[52] **U.S. Cl.** **395/750**; 395/348

[58] **Field of Search** 395/750, 159; 364/707

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[57] **ABSTRACT**

A computer system is disclosed comprising a clock generator circuit having a clock speed register and circuitry for generating a processor clock signal at a frequency determined by the clock speed register, wherein the processor executes a performance manager program that writes the clock speed register according to a performance state selected by an application program. The application program selects the performance state to maximize performance during processor intensive functions and to maximize power conservation during interactive functions.

15 Claims, 6 Drawing Sheets